IN THE CLAIMS:

1. (Original) A semiconductor device, comprising:

a bulk substrate;

a multiple thickness buried oxide layer formed above said bulk substrate; and

an active layer formed above said multiple thickness buried oxide layer, said semiconductor device being formed in said active layer above said multiple thickness buried oxide layer.

2. (Original) The device of claim 1, wherein said bulk substrate is comprised of silicon.

3. (Original) The device of claim 1, wherein said semiconductor device is a transistor.

4. (Original) The device of claim 1, wherein said semiconductor device is part of at least one of a microprocessor, a memory device and a logic device.

5. (Original) The device of claim 1, wherein said active layer is comprised of silicon.

6. (Original) The device of claim 1, wherein said active layer has a thickness ranging from approximately 5-30 nm.

7. (Original) The device of claim 1, wherein said buried oxide layer is comprised of silicon dioxide.

8. (Original) The device of claim 1, wherein said multiple thickness buried oxide layer comprises:

a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections.

9. (Original) The device of claim 1, wherein said semiconductor device is a transistor having a channel region, at least a portion of said channel region being positioned above a section of said buried oxide layer that has a thickness that is less than a thickness of a remaining portion of said buried oxide layer.

10. (Original) The device of claim 1, wherein said semiconductor device is a transistor comprised of a gate electrode and wherein said multiple thickness buried oxide layer has a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than a thickness of said second sections, said first section being at least partially positioned under said gate electrode.

11. (Original) The device of claim 1, wherein said semiconductor device is a transistor comprised of a gate electrode and wherein said multiple thickness buried oxide layer

has a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than a thickness of said second sections, said first section being substantially aligned with said gate electrode.

12. (Original) The device of claim 8, wherein said first section has a thickness ranging from approximately 30-50 nm and said second sections have a thickness ranging from approximately 120-180 nm.

13. (Original) A transistor, comprising:

a bulk substrate;

a buried oxide layer formed above said bulk substrate, said buried oxide layer comprising a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections; and

an active layer formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer.

14. (Original) The device of claim 13, wherein said bulk substrate is comprised of silicon.

15. (Original) The device of claim 13, wherein said transistor is part of at least one of a microprocessor, a memory device and a logic device.

16. (Original) The device of claim 13, wherein said active layer is comprised of silicon.

17. (Original) The device of claim 13, wherein said active layer has a thickness ranging from approximately 5-30 nm.

18. (Original) The device of claim 13, wherein said buried oxide layer is comprised of silicon dioxide.

19. (Original) The device of claim 13, wherein said transistor comprises a channel region, at least a portion of said channel region being positioned above at least a portion of said first section of said buried oxide layer.

20. (Original) The device of claim 13, wherein said transistor comprises a gate electrode and wherein said first section of said buried oxide layer is at least partially positioned under said gate electrode.

21. (Original) The device of claim 13, wherein said transistor comprises a gate electrode and wherein said first section of said buried oxide layer is substantially aligned with said gate electrode.

22. (Original) The device of claim 13, wherein said first section has a thickness ranging from approximately 30-50 nm and said second sections have a thickness ranging from approximately 120-180 nm.

23. (Original) A transistor comprised of a channel region, said transistor comprising:

a bulk silicon substrate;

a buried oxide layer formed above said bulk silicon substrate, said buried oxide layer comprising a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections; and

an active layer formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer, at least a portion of said channel region being positioned above said first section of said buried oxide layer.

24. (Original) The device of claim 23, wherein said transistor is part of at least one of a microprocessor, a memory device and a logic device.

25. (Original) The device of claim 23, wherein said active layer is comprised of silicon.

26. (Original) The device of claim 23, wherein said active layer has a thickness ranging from approximately 5-30 nm.

27. (Original) The device of claim 23, wherein said buried oxide layer is comprised of silicon dioxide.

28. (Original) The device of claim 23, wherein said transistor further comprises a gate electrode and wherein said first section of said buried oxide layer is at least partially positioned under said gate electrode.

29. (Original) The device of claim 23, wherein said transistor further comprises a gate electrode and wherein said first section of said buried gate oxide layer is substantially aligned said gate electrode.

30. (Original) The device of claim 23, wherein said first section has a thickness ranging from approximately 30-50 nm and said second sections have a thickness ranging from approximately 120-180 nm.

31.-48. (Canceled)